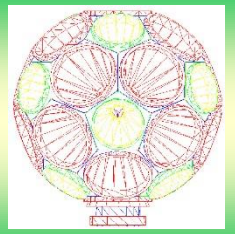
MIND



Massively Interconnected NoDe

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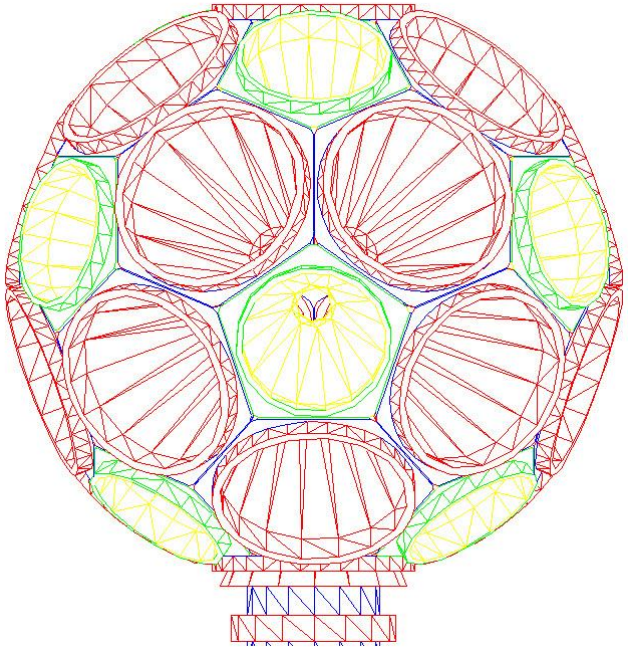
Outline



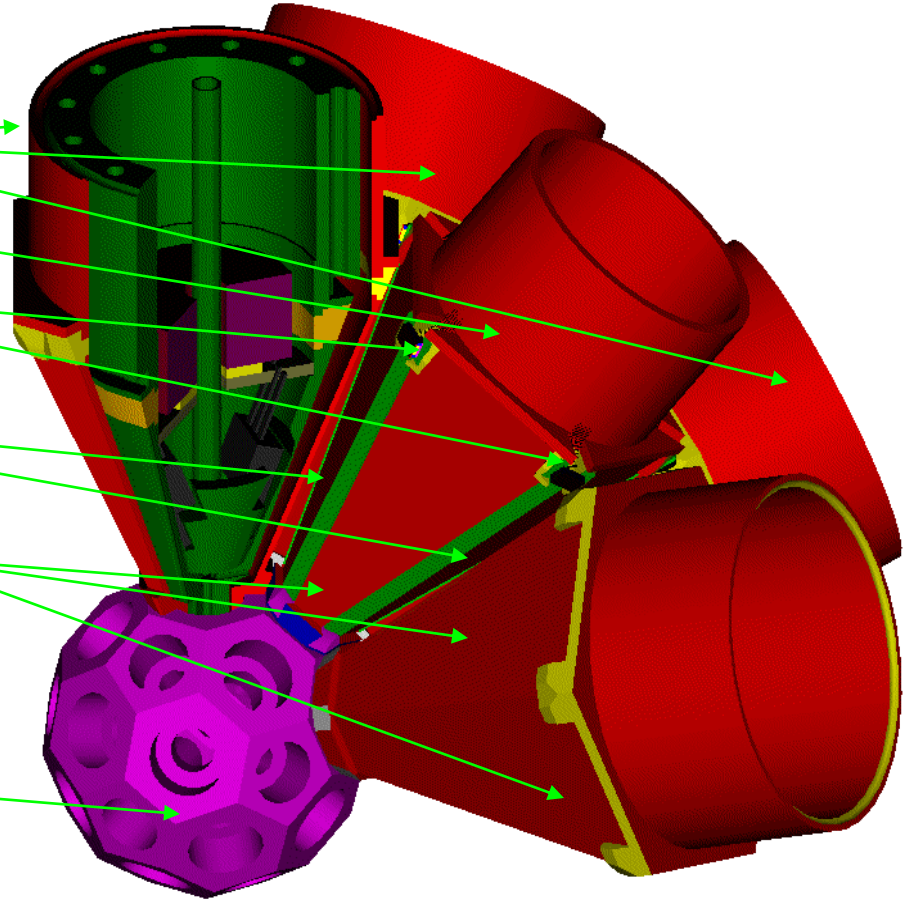
- Summary
- Conceptual Description
- Performance
- Applications

Summary

- The proposed computing architecture is capable of:
  - 20 Trillions 98-bit Multiply-Accumulate (TMAC) operations per second or
  - 12 Trillions Core I7 instructions per second (TMIP) or
  - Equivalent combination of TMACs and TMIPs
  - Communication bandwidth
    - Internal - 25 Tb/sec
    - External – 4 Tb/sec
- The above level of performance is delivered in 2 Liters volume that also includes secondary power supplies, cooling subsystem and all required internal and external interconnects

Mechanical Superstructure

- Integrated Processing Power Supply and Cooling Modules - IPPCMs
- Truncated Icosahedron topology
  - 20 hexagonal IPPCMs
  - 12 pentagonal IPPCMs
- High-Density External Optical Interconnects
- Free-Space internal Optical Interconnects
- 2,000cm^2 of die attach area in 2 Liters volume
- Common conductive Icosahedral Core



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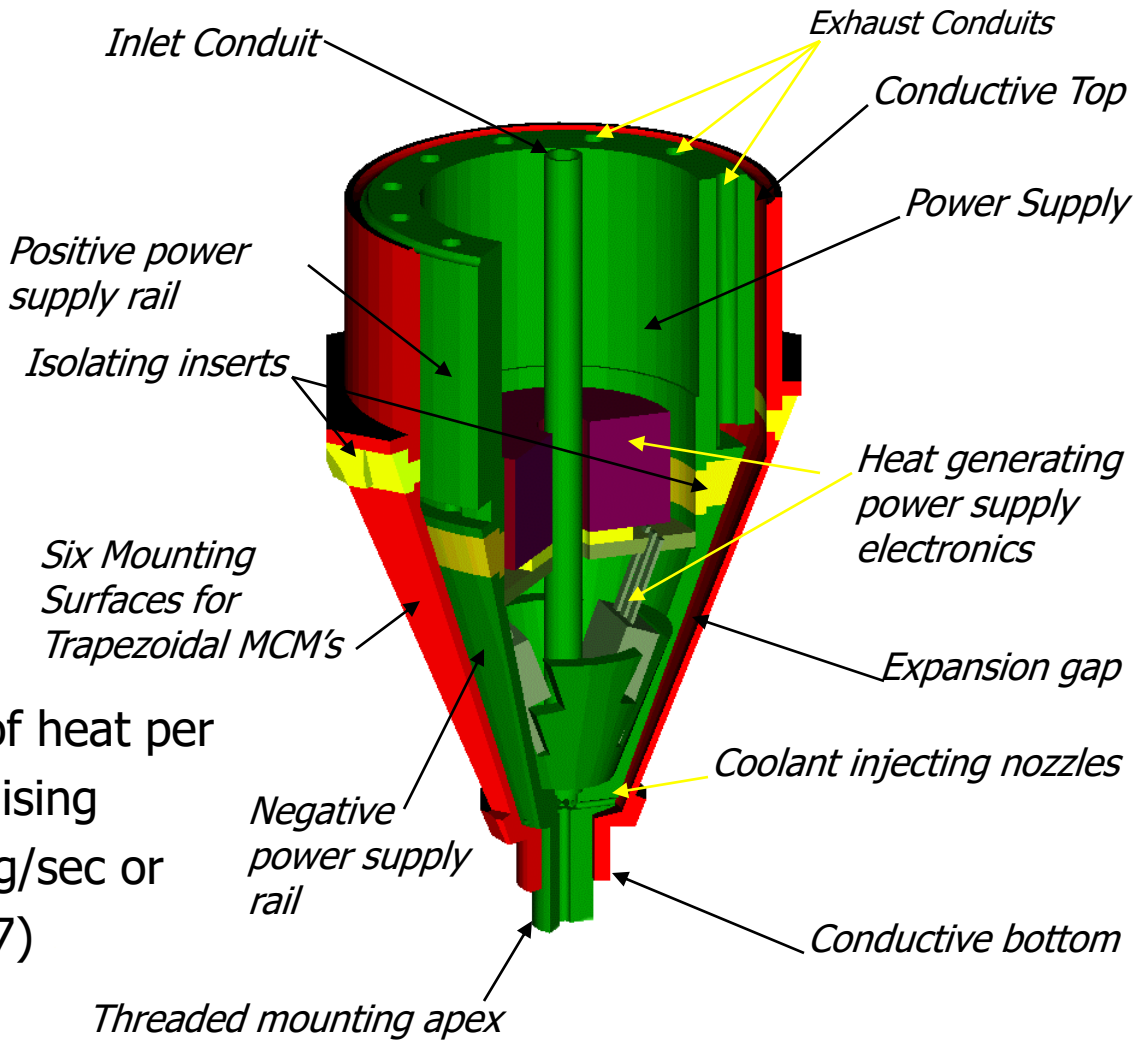
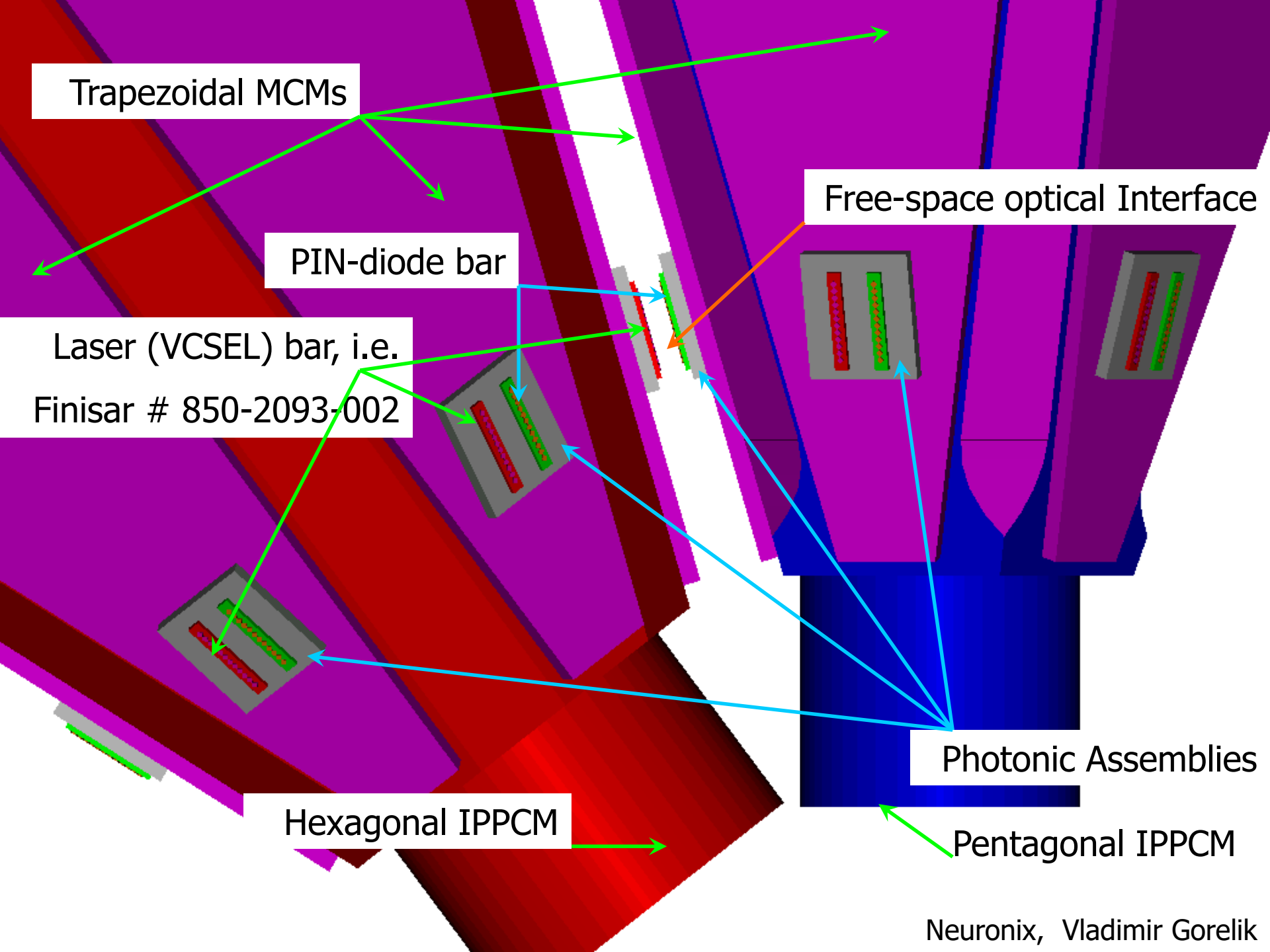
Integrated Processing Power Supply and Cooling Module (IPPCM)

- Two types of IPPCMs:
  - Pentagonal
  - Hexagonal (shown)
- Coaxial topology:
  - Local Power Supply with low-inductance power rails.
  - Local Cooling capable of dissipating up to 500W of heat per IPPCM without compromising photonic components (6g/sec or 2.4cm^3/sec of 3M's FC-77)





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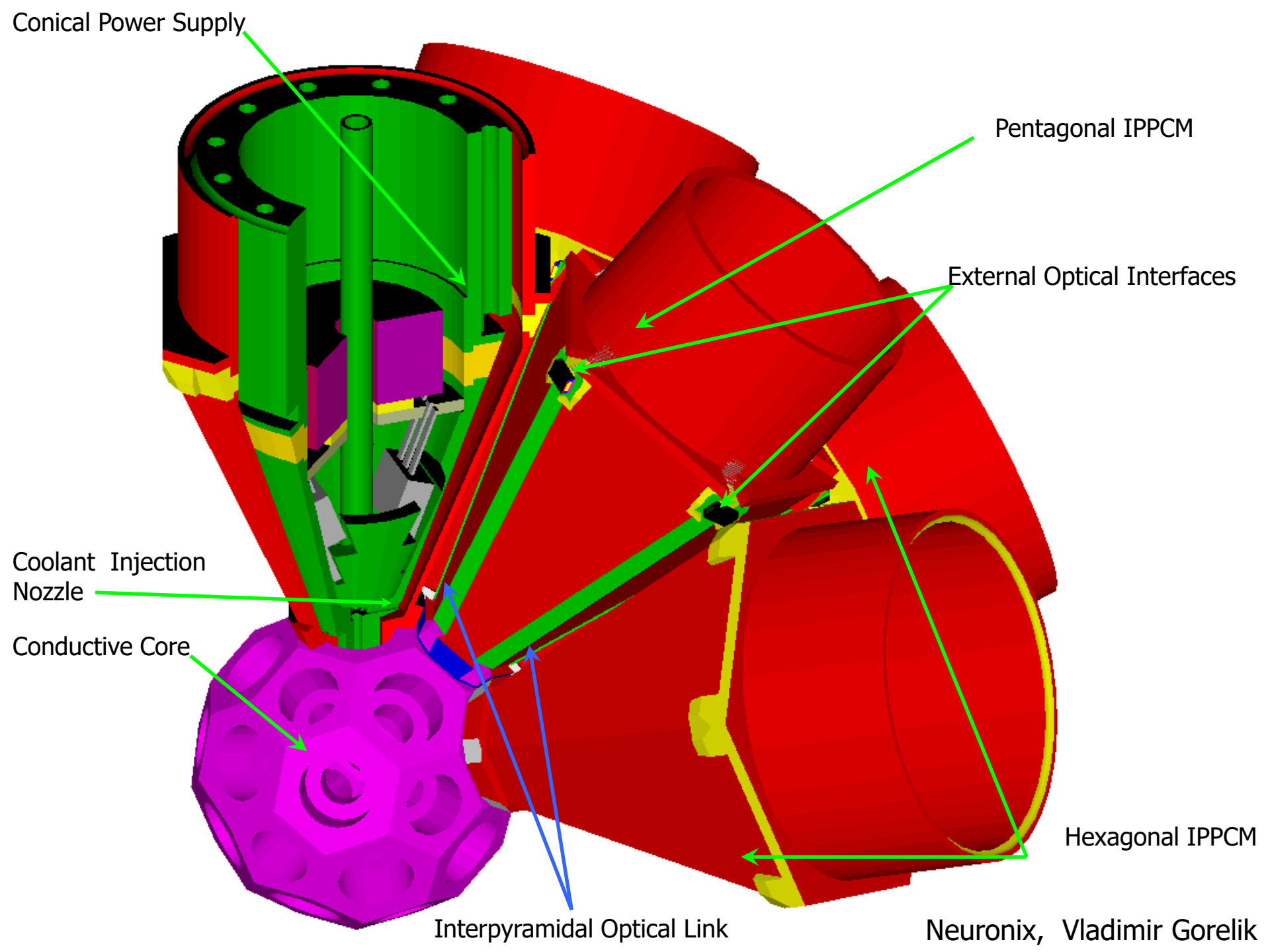

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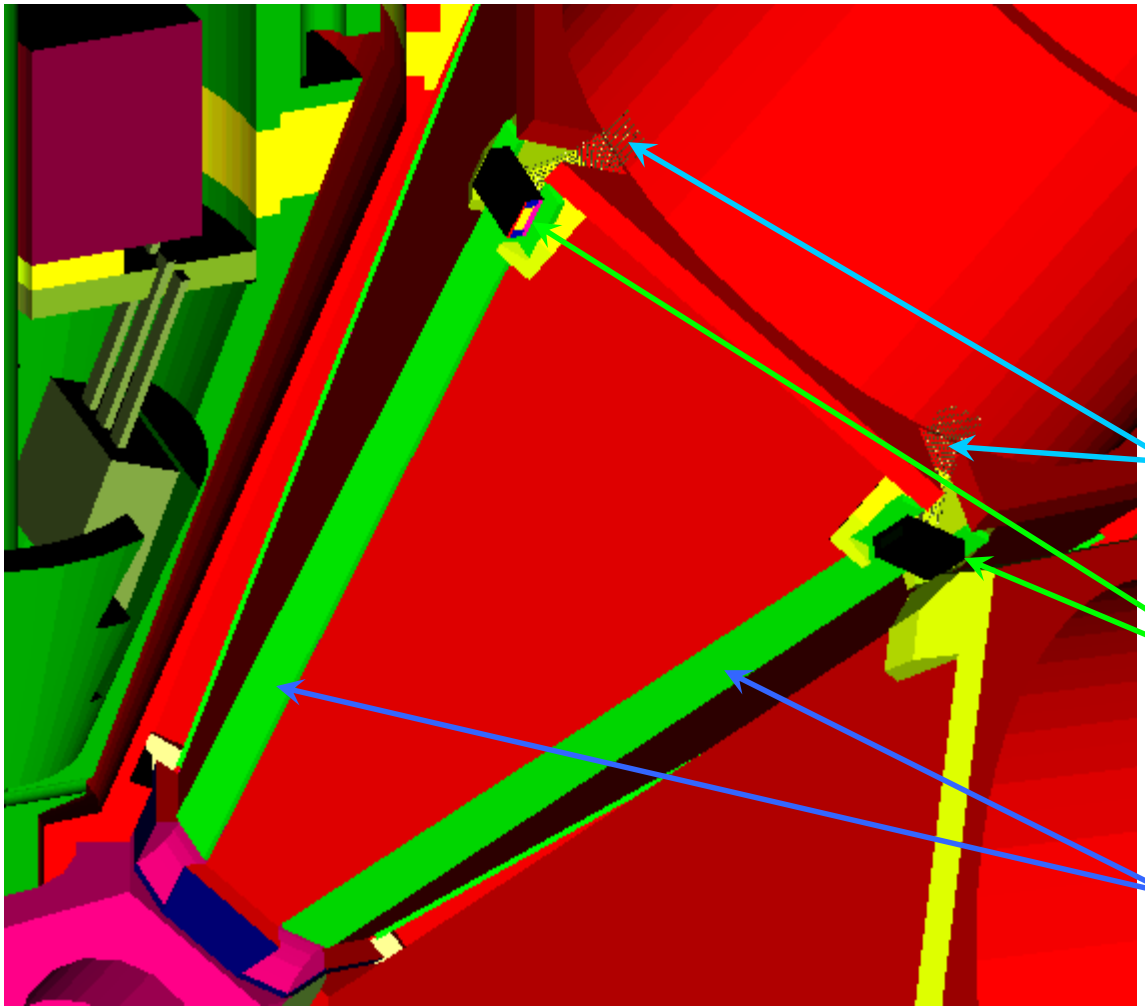
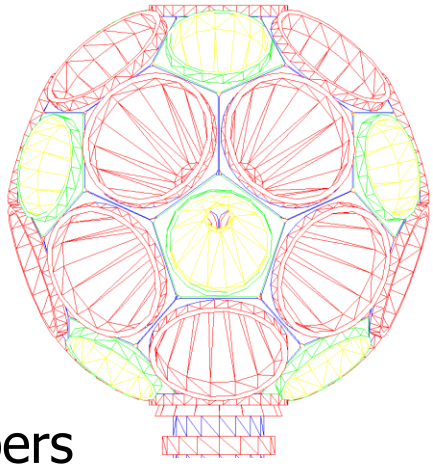
External Optical Interconnect





Optical Fibers

Photonic Assemblies

Photonic MCMs

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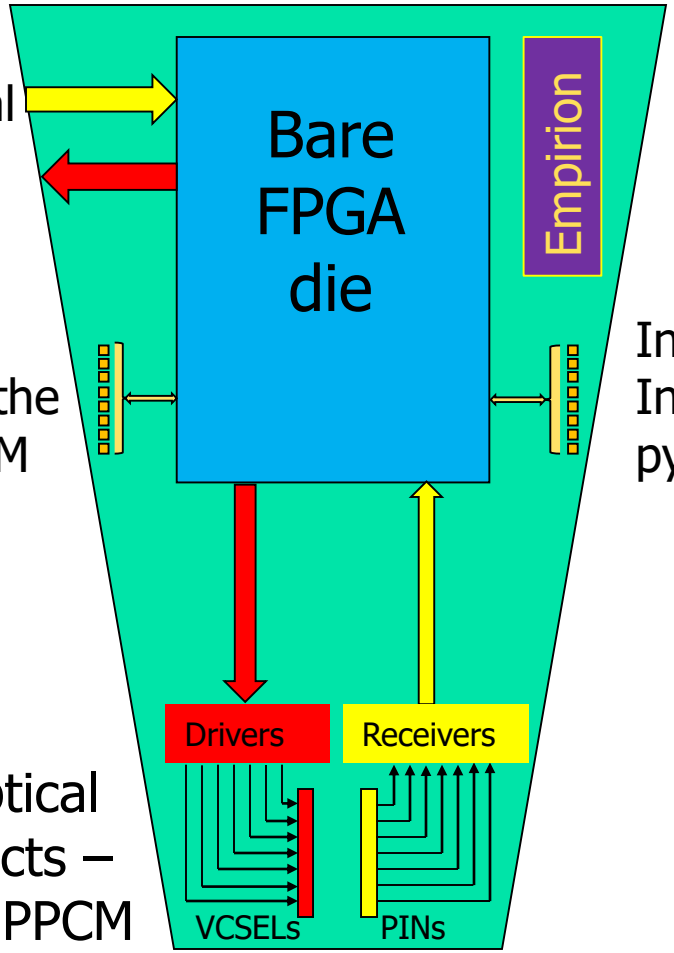
TPM Layout



External optical Interconnects

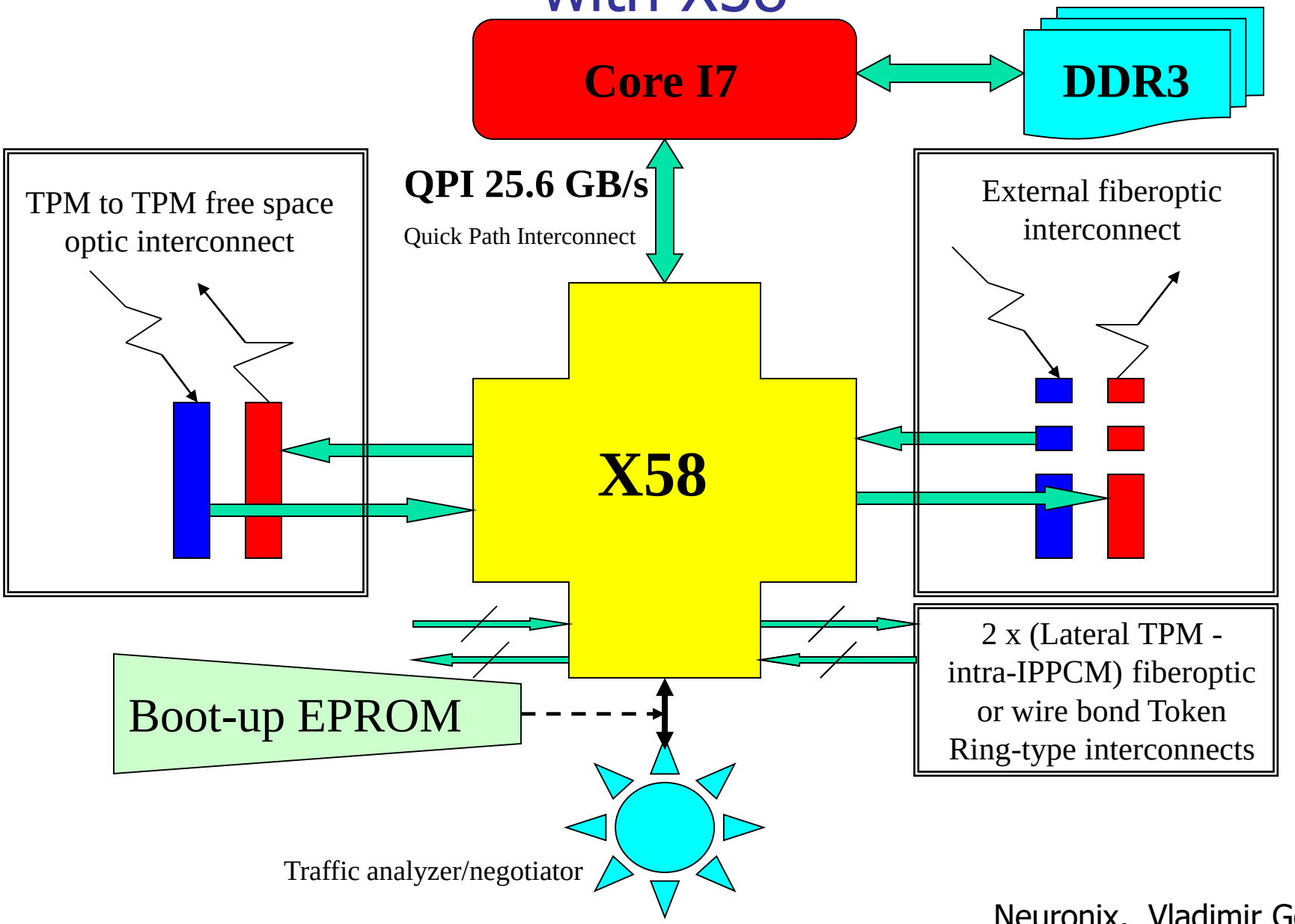
Internal lateral Interconnects within the pyramid – TPM-to-TPM

Internal lateral Interconnects within the pyramid – TPM-to-TPM

Internal optical Interconnects – IPPCM-to-IPPCM

180 Identical TPMs per complete MIND

TPM-diagram modified for MIND Core I7 with X58



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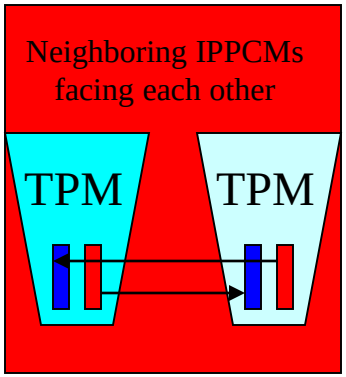
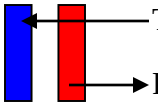
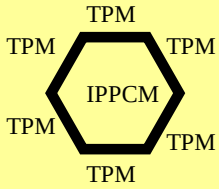
Richness and Complexity of MIND Interconnects





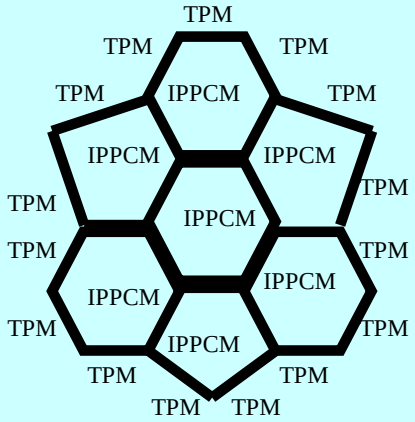
Zero-Level (no protocol overhead is required)

Comm. Ring connecting all TPMs on each IPPCM



Multiple levels of protocols with specialized headers are circulating in this Comm. Ring

Communication Ring connecting all TPMs on each IPPCM



-A single Near-Neighbor cluster centered around a hexagonal IPPCM.

-Similar clusters are associated with each hexagonal and pentagonal IPPCM.

-A simple routing scheme exists between all TPM.

First-Level protocol:

- See Notes below for explanation

Second-Level protocol:

- See Notes below for explanation
- Some external interconnect fibers may be routed into a distant IPPCMs for non-negotiable and very fast data transfer.
- Some clusters may contain a memory-only pyramidal module in its center offering large storage capacity to the surrounding IPPCMs

Third-Level protocol – see next slide

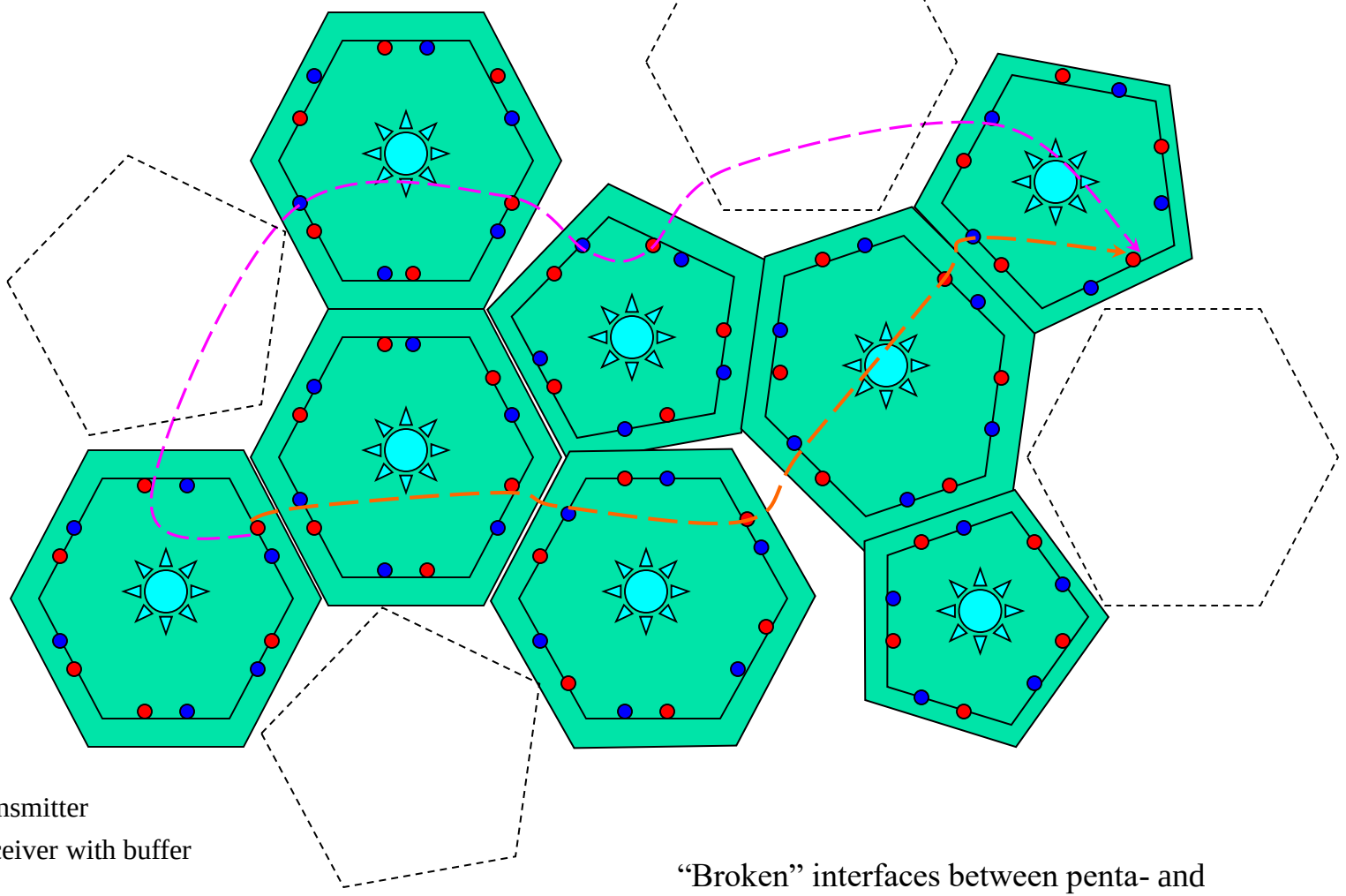
Slide glossary:

TPM – Trapezoidal Processing and Local Memory Module

IPPCM – Integrated Processing, Power supply and Cooling Module

Comm. RING – A communication link that locally and serially interconnects all *TPM*s around the circumference of each *IPPCM*. This structure is not for payload transfer – instead, it is primarily used for establishing/negotiating an optimal communication route across a closed-loop truncated icosahedral network of *TPM* nodes.

Traffic negotiation and routing schemes



Optical Transmitter

Optical Receiver with buffer

Hexagonal and Pentagonal Communication rings

Traffic analyzer/negotiator – one per TPM, six or five per IPPCM

"Broken" interfaces between penta- and hexagons are due to the inability to map an icosahedral (spherical) surface on a 2D sheet.

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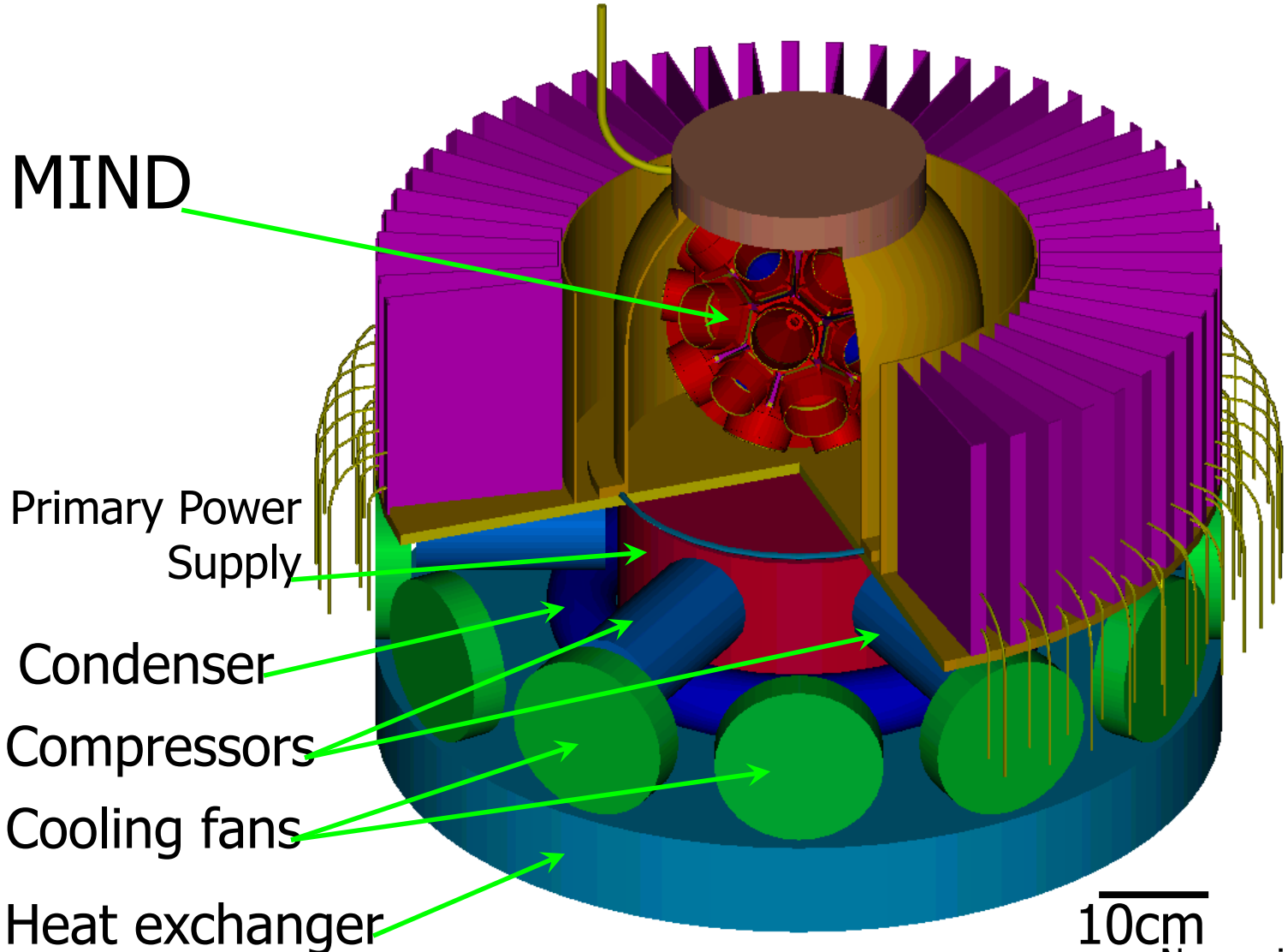
MIND – Massively Interconnected NoDe



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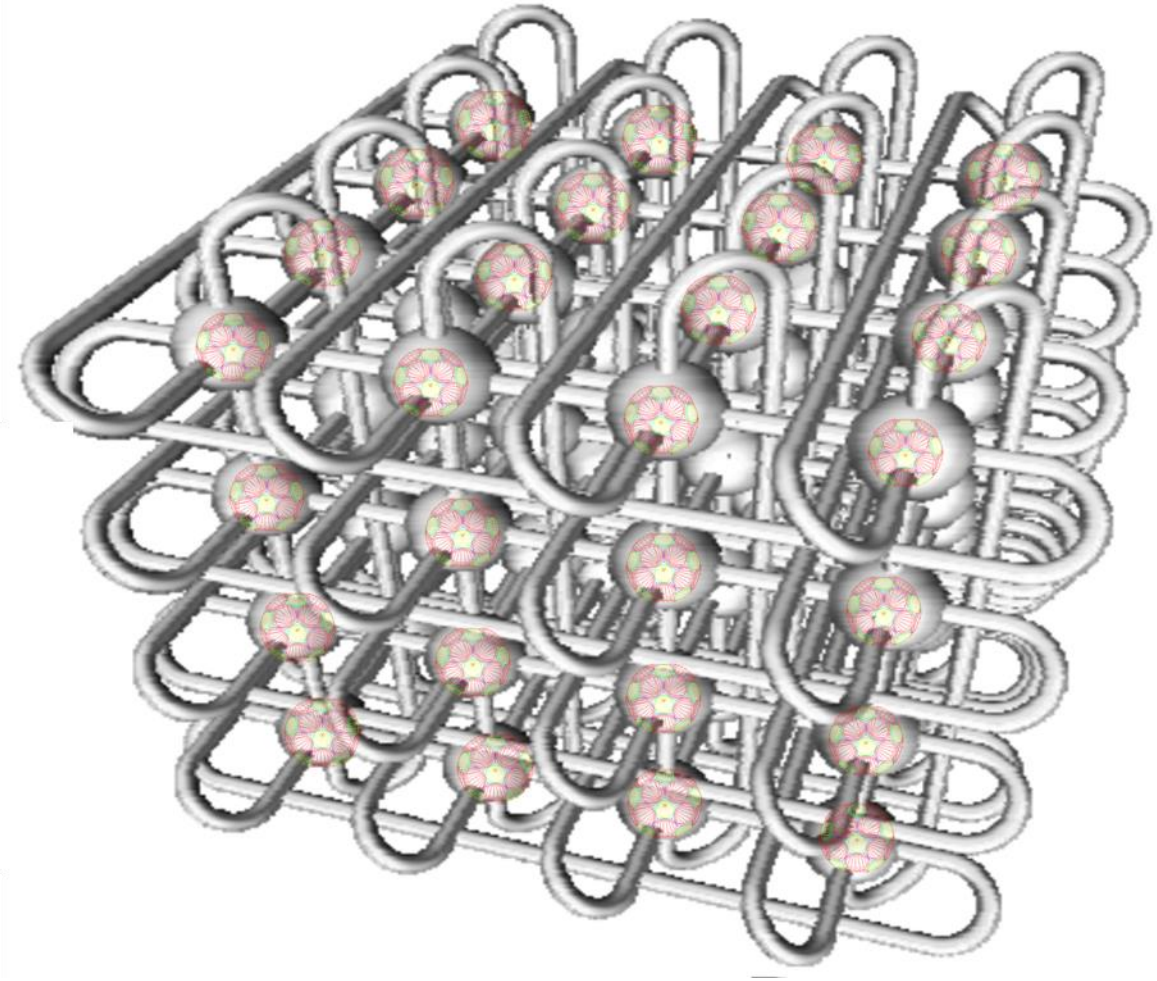
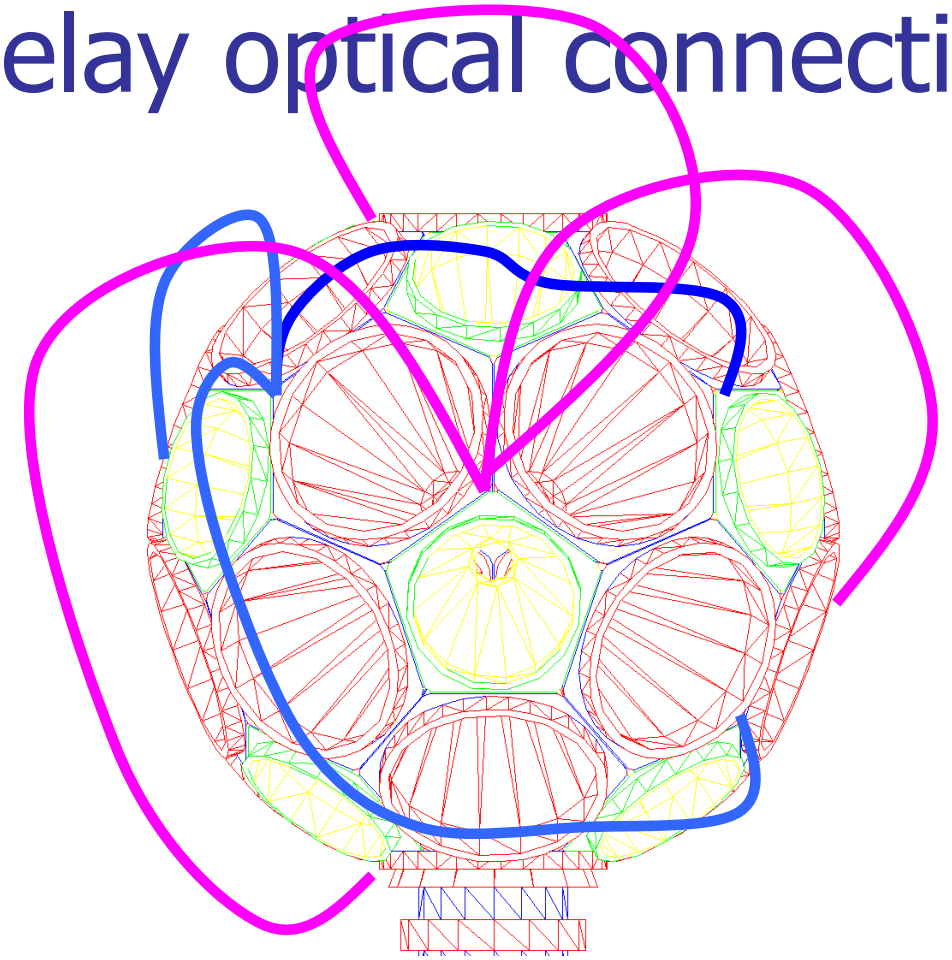
Hypercube with MIND in each node



Packaging density by much exceeds Fujitsu 6D Torus as each node contains up to 180 100Gb/sec optical interconnects – 18Tbits/sec per node

Long-range, low Latency and Low Delay optical connections



Optical fibers connecting Far Neighbors establish either direct routes or run via an optical switch for added flexibility with virtually no delay and overhead

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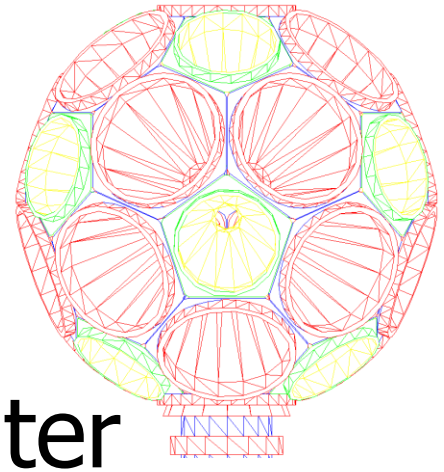
Example of MIND Performance Metrics

including all processing, secondary power supply, cooling and interconnect components

Device	Unitary Performance Of a single component				MIND Performance In a 2 Liter volume			
	GMAC	DMIPS	IO [Gb /sec]	Power [W]	GMAC	DMIPS	IO	W
XC5VSX240T	700	N/A	90	47	126000	N/A	16200	8460
XC5VFX200T	170	2000	156	47	30600	360K	26080	8460
Intel Core I7 Extreme with X58	N/A	76383	25.6	200	N/A	13748940	4608	36000[1]

[1] This level of power consumption would require more potent then FC-77 coolant (Freon-12 ?)

Applications



- Supercomputing
- Intelligent Network-Switch/Router
- Neural Networks
- Intelligent Control Agents
- Robotics
- Borg

Follow up with Altera Factory Apps

- The concept was developed over ten years ago; deemed a "blue-sky research" and unrealistic by my employer at the time due to the complexity and an absence of an industry partner and a "champion." OpenCL and SDSoC from Xilinx vastly improved FPGA tools and IP.
- Traditional HPC derived applications
  - Fluid dynamics
  - FEA
  - Protein folding
  - Data mining
- Not-traditional
  - Cortical Processor
- Funding:
  - DARPA Cortical processor or similar
  - Department of Energy – HPC
  - Internal Altera
  - External investors